

● PRINTER RUSH ●

(PTO ASSISTANCE)

Application : <u>09/427649</u>	Examiner : <u>Quach</u>	GAU : <u>2826</u>
From : <u>LH</u>	Location : <u>IDC</u> FMF FDC	Date : <u>5-18-05</u>
Tracking #: <u>06084975</u>		Week Date: <u>3-14-05</u>

DOC CODE	DOC DATE	MISCELLANEOUS
<input type="checkbox"/> 1449	_____	<input type="checkbox"/> Continuing Data
<input type="checkbox"/> IDS	_____	<input type="checkbox"/> Foreign Priority
<input type="checkbox"/> CLM	_____	<input type="checkbox"/> Document Legibility
<input type="checkbox"/> IIFW	_____	<input type="checkbox"/> Fees
<input type="checkbox"/> SRFW	_____	<input type="checkbox"/> Other
<input type="checkbox"/> DRW	_____	
<input type="checkbox"/> OATH	_____	
<input checked="" type="checkbox"/> 312	<u>2/28/02</u>	
<input type="checkbox"/> SPEC	_____	

[RUSH] MESSAGE: 1) Amendment dated (2/28/02) contains illegible
dated on pages 1 and 2.
 Please resolve

Thank you

LH

[XRUSH] RESPONSE: Corrected

Adrian Lee
Gregory Taylor (501)-533-9800 INITIALS: PS

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.

REV 10/04

5/24

09/627,649

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PATENT APPLICATION
Docket No. 11675.76.3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Sandhu et al.

Serial No.:

09/627,649

Filed:

July 28, 2000

For:

INTERLEVEL DIELECTRIC STRUCTURE

Examiner:

T. Quach

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) Art Unit
) 2814
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)AMENDMENT AND RESPONSECommissioner for Patents
Washington, D. C. 20231

Sir:

In response to the Office Action mailed from the United States Patent and Trademark Office on August 29, 2001, please enter the following amendments and remarks into the file of the above-identified application.

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 2, line 2 with the following rewritten paragraph:

-- This application is a divisional application of United States Patent Application Serial No. 08/677,514, filed on July 10, 1996, now United States Patent No. 6,107,183, which is incorporated herein by reference. --

Please replace the paragraph beginning at page 3, line 6 with the following rewritten paragraph:

-- One way to decrease unneeded capacitance between metal lines in an integrated circuit is to decrease the dielectric constant of the material between them. Silicon dioxide, the material of choice for interlevel dielectrics, has a relatively high dielectric constant. Replacing silicon dioxide with a material having a lower dielectric constant would thus provide reduced capacitance. Useable materials having a low dielectric constant (e.g. less than about 3.6.) are generally much less stable than silicon dioxide and are thus unable to reliably protect the metal lines, and are unable to withstand further processing. --

Please replace the paragraph beginning at page 3, line 13 with the following rewritten paragraph:

-- One way to gain some of the benefits of low dielectric constant materials is shown in Figure 1. Figure 1 is a partial cross section of a partially formed integrated circuit device. A substrate or lower layer 12 has a first dielectric layer 14 comprised of a traditional dielectric material such as silicon dioxide. Lines of conductive material 16, typically metal, overlie first dielectric layer 14. A material with a dielectric constant lower than that of silicon dioxide 18 is located in between lines of conductive material 16. Lines of conductive material 16 together with low dielectric constant dielectric material 18 are covered by a

second dielectric layer 21 comprised of a traditional dielectric material such as silicon dioxide. Second dielectric layer 21 together with first dielectric layer 14 isolate low dielectric constant dielectric material 18 from other portions of the integrated circuit. Second dielectric layer 21 allows further processing, including formation of contact holes for contacting lines of conductive material 16 such as contact hole 46, without exposing dielectric material 18 to processing agents. --

Please replace the paragraph beginning at page 5, line 2 with the following rewritten paragraph:

-- In accordance with the present invention, an interlevel dielectric structure includes first and second dielectric layers between which are located lines of a conductive material with a dielectric material in spaces between the lines of conductive material, with the lower surface of the dielectric material extending lower than the lower surface of lines of conductive material adjacent thereto, and the upper surface of the dielectric material extending higher than the upper surface of lines of conductive material adjacent thereto, thus reducing fringe and total capacitance between the lines of conductive material. The dielectric material, which has a dielectric constant of less than about 3.6, does not extend directly above the upper surface of the lines of conductive material, allowing formation of subsequent contacts down to the lines of conductive material without exposing the dielectric material to further processing. --